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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,299	05/04/2006	Hazuki Okabayashi	P29851	6791

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EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
12/28/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com
pto@gbpatent.com

Office Action Summary	Application No.	Applicant(s)	
	10/578,299	OKABAYASHI ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/4/06; 9/13/06; 07/06/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The Oath/Declaration filed on May 4, 2006 has been considered.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on August 4, 2006 and July 6, 2007 is being considered by the examiner. However, several Japanese documents are listed on the IDS but not submitted. These documents have not been considered.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-8 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent Application No. 10/577,133 and claims 1-8 of U.S. Patent Application No. 10/583,773. Although the conflicting claims are not identical, they are not patentably distinct from each other as shown below.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

The following table is provided simply for illustrative purposes.

Instant Application: 10/578,299	Application No. 10/577,133	Application No. 10/583,773
Claim 1. A cache memory comprising: an addition unit operable to add, to each cache entry holding line data, a caching termination attribute indicating whether or not caching of the cache entry is allowed to be terminated; a selection unit	**Claim 10.** A cache memory which holds, for each cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the order, the cache entry holding unit data for caching, said cache memory comprising:	A cache memory comprising: a flag holding unit which holds, in a correspondence with a cache entry which holds a data unit of caching, a valid flag indicating whether or not the

operable to select a cache entry that has been added with a caching termination attribute indicating that caching is allowed to be terminated, and has been set with a dirty flag indicating that the cache entry has been written into; and a write back unit operable to write back, to a memory, line data of the selected cache entry, regardless of an occurrence of a cache miss.	A modification unit operable to modify the order data regardless of an actual access order; and A selection unit operable to select, based on the modified order data, a cache entry to be replaced.	cache entry is valid, and a dirty flag indicating whether or not the cache entry has been written into; a command holding unit which holds a command issued by a processor; and an altering unit operable to alter, based on a command held by said command holding unit, at least one of the valid flag and the dirty flag, contrary to the state of the cache entry.

5. Claims 1-10 of U.S. Patent Application No. 10/577,133 and claims 1-8 of U.S. Patent Application No. 10/583,773 contain every element of claims 1-8 of the instant application and as such anticipate claims 1-8 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 5, 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Masatoshi (JP 06-309231).

As per claim 1, MASATOSHI discloses a cache memory comprising: an addition unit operable to add, to each cache entry holding line data, a caching termination attribute indicating whether or not caching of the cache entry is allowed to be terminated [Fig. 1; pars. 0018, 0021, 0022, 0023]; a selection unit operable to select a cache entry that has been added with a caching termination attribute indicating that caching is allowed to be terminated, and has been set with a dirty flag indicating that the cache entry has been written into [pars. 0019, 0021-0023]; and a write back unit operable to write back, to a memory, line data of the selected cache entry, regardless of an occurrence of a cache miss [Abstract; par. 0020].

As per claim 2, MASATOSHI discloses said adding unit includes: a holding unit operable to hold an address range specified by a processor; a search unit operable to search for a cache entry holding line data within the address range held in said holding unit [par. 0018]; and a setting unit operable to set, to the searched-out cache entry, the

caching termination attribute indicating that caching is allowed to be terminated [Abstract].

As per claim 5, though MASATOSHI discloses said addition unit includes: an instruction detection unit operable to detect execution, by a processor, of a store instruction having, as instruction details, addition of the caching termination attribute indicating that caching is allowed to be terminated, and writing of data [pars. 0021-0023]; and a setting unit operable to set the caching termination attribute to a cache entry that has been written into in accordance with the detected instruction [Fig. 1, S1-S8].

As per claim 6, MASATOSHI discloses said write back unit is operable to write back data of a cache entry to the memory, when a memory bus has an idle cycle [par. 0019].

As per claim 8, the rationale in the rejection of claim 1 is herein incorporated.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masatoshi (JP 06-309231) in view of Yasuto (JP 08-069417).

As per claim 3, MASATOSHI discloses said search unit includes: a first conversion unit operable, in the case where a start address of the address range held in said holding unit indicates a point midway through line data, to convert the start address into a start line address indicating a start line included in the address range [par. 0020];

Though MASATOSHI discloses converting the start address into a start line address indicating a start line included in the address range, MASATOSHI does not explicitly disclose a second conversion unit operable, in the case where an end address of the address range held in said holding unit indicates a point midway through line data, to convert the end address into an end line address indicating an end line included in the address range; and a judgment unit operable to judge whether or not there exist cache entries holding data corresponding to respective line addresses from the start line address to the end line address.

YASUTO discloses a second conversion unit operable, in the case where an end address of the address range held in said holding unit indicates a point midway through line data, to convert the end address into an end line address indicating an end line included in the address range [Abstract]; and a judgment unit operable to judge whether or not there exist cache entries holding data corresponding to respective line addresses

from the start line address to the end line address [Abstract] to improve the performance of a computer system by preventing unnecessary writing to a memory block of low-order level (Abstract).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the system of MASATOSHI to include converting the end address into an end line address indicating an end line included in the address range and judging whether or not there exist cache entries holding data corresponding to respective line addresses from the start line address to the end line address since this would have improved the performance of a computer system by preventing unnecessary writing to a memory block of low-order level (Abstract) as taught by YASUTO.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masatoshi (JP 06-309231) in view of Tamotsu (JP 61-016348).

As per claim 4, though MASATOSHI discloses the cache entry that has been added with the caching termination attribute indicating that caching is allowed to be terminated, MASATOSHI does not explicitly teach a replacement unit operable, when a cache miss occurs, to select, as a subject for replacement, the cache entry that has been added with the caching termination attribute indicating that caching is allowed to be terminated.

TAMOTSU discloses a replacement unit operable, when a cache miss occurs, to select, as a subject for replacement, the cache entry that has been added with the caching termination attribute indicating that caching is allowed to be terminated [Abstract] to reduce the overhead for expulsion of old blocks from a buffer memory at a block replacement time (Abstract).

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of MASATOSHI to include a replacement unit operable, when a cache miss occurs, to select, as a subject for replacement since this would have been able to reduce the overhead for expulsion of old blocks from a buffer memory at a block replacement time (Abstract).

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masatoshi (JP 06-309231) in view of Pateru et al. (JP 09-259036).

As per claim 7, though Masatoshi discloses each cache entry has a dirty flag and a write back unit to write back to the memory the cache entry selected by the selection unit, MASATOSHI does not explicitly teach each cache entry has a dirty flag for each of a plurality of sub-lines making up one line, and said write back unit is operable to write back, to the memory, only a dirty sub-line.

PATERU discloses each cache entry has a dirty flag for each of a plurality of sub-lines making up one line, and said write back unit is operable to write back, to the

memory, only a dirty sub-line [Abstract] in order to maintain consistency inside a write-back cache memory (Abstract).

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of MASATOSHI to include with each cache entry a dirty flag for each of a plurality of sub-lines making up one line, and a write back unit operable to write back, to the memory, only a dirty sub-line as taught by PATERU since this would have facilitated maintaining consistency inside a write back cache memory (Abstract).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JP 2001-005725 discloses said addition unit includes: an instruction detection unit operable to detect execution, by a processor, of a store instruction having, as instruction details, addition of the caching termination attribute indicating that caching is allowed to be terminated [Abstract].

TAMOTSU discloses a cache memory with an addition unit where each cache entry holds a cache termination attribute indicating if the cache entry is allowed to be terminated, and a selection unit selecting a cache entry that has been added with the caching termination attribute.

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

14. When responding to the Office action, Applicant is also advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached Monday to Friday, from 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached Monday to Friday, at (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

December 14, 2007

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
12/20/07

Mardochee Chery
Examiner
AU: 2188